second output driver circuitry to output data onto a first external signal line wherein:

the second output driver circuitry outputs a first portion of data in response to a rising edge transition of a first external clock signal and the second output driver circuitry outputs a second portion of data in response to a falling edge transition of the first external clock signal.

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22 18

~~172~~. (Amended) The integrated circuit device of claim ~~168~~ wherein [the] a clock alignment circuit generates an internal clock signal, and the first output driver circuitry and the second output driver circuitry output [outputs] data in response to the internal clock signal.

In claim 174, lines 3, 7, and 11, before "output" insert --first--.

In claim 175, line 5, before "output" insert --first--.

In claim 176, line 4, before "output" insert --first--.

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27 24

~~177~~. (Amended) The integrated circuit device of claim ~~174~~ [176] further including a clock alignment circuit [coupled to the first external clock signal, the clock alignment circuit] to generate a first internal clock signal using the first external clock signal, wherein the multiplexer circuitry couples the first portion of data to the input of the first output driver circuitry in response to the first internal clock signal.
